Cont D1 Sub E1

proportional to a square of a ratio of the second resistance and the first resistance.

D2

10. (Amended) An integrated circuit voltage ramp generator according to Claim 9, wherein said charging circuit comprises a degenerate current mirror circuit.

11. (Amended) An integrated circuit voltage ramp generator according to Claim 10, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

12. (Amended) An integrated circuit voltage ramp generator according to Claim 11, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

13. (Amended) An integrated circuit voltage ramp generator according to Claim 9, wherein said capacitance comprises a gate capacitance of a MOS transistor.

14. (Amended) An integrated circuit voltage ramp generator according to Claim 9, wherein current generated by

said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

15. (Twice Amended) An integrated circuit voltage ramp generator comprising:

a semiconductor substrate;

a capacitance on said semiconductor substrate; and

a charging circuit on said semiconductor substrate and connected to said capacitance and comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance.

17. (Amended) An integrated circuit voltage ramp generator according to Claim 15, wherein said degenerate

current mirror circuit comprises:

Cont D4

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

18. (Amended) An integrated circuit voltage ramp generator according to Claim 17, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

19. (Amended) An integrated circuit voltage ramp generator according to Claim 15, wherein said capacitance comprises a gate capacitance of a MOS transistor.

20. (Amended) An integrated circuit voltage ramp generator according to Claim 15, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a

Cont D4

reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

D5

21. (Twice Amended) An integrated circuit current ramp generator comprising:

a semiconductor substrate;

a voltage ramp generator on said semiconductor substrate and comprising

a capacitance, and

a charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

a conversion circuit on said semiconductor substrate and connected to said voltage ramp generator for generating a current ramp.

D6

22. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said conversion circuit comprises a third resistance.

23. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said third resistance

Cmt D6

comprises an implanted resistance having a positive temperature coefficient.

Sub E4

24. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said charging circuit comprises a degenerate current mirror circuit on said semiconductor substrate.

25. (Amended) An integrated circuit current ramp generator according to Claim 24, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

26. (Amended) An integrated circuit current ramp generator according to Claim 25, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

27. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said capacitance comprises a gate capacitance of a MOS transistor.

28. (Amended) An integrated circuit current ramp

Cont D6

generator according to Claim 21, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

D7

Sub E5

29. (Twice Amended) An integrated circuit current ramp generator comprising:

a semiconductor substrate;

a voltage ramp generator on said semiconductor substrate and comprising

a capacitance having a first resistance, and

a charging circuit connected to said capacitance and comprising

a current generator, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance; and

Cont D1 Sub E6

a third resistance on said semiconductor substrate and connected to said voltage ramp generator for generating a current ramp.

D8

31. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein said third resistance comprises an implanted resistance having a positive temperature coefficient.

32. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

33. (Amended) An integrated circuit current ramp generator according to Claim 32, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

34. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein said capacitance comprises a gate capacitance of a MOS transistor.

Cont D8

35. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

D9

Sub E7

36. (Twice Amended) A method for generating a ramp voltage comprising:

generating a capacitance charging current using an integrated circuit charging circuit comprising a semiconductor substrate, and a current generator on the semiconductor substrate and having a first resistance and a circuit on the semiconductor substrate and connected to the generator having a second resistance for enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

charging a capacitance on the semiconductor substrate with the capacitance charging current for generating the ramp voltage.

D10 Sub E7

37. (Amended) A method according to Claim 36, wherein the circuit comprises a degenerate current mirror